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KESTX03

400MHz - 460MHz ASK Transmitter

Target Specification

DS4820 - 1.6 August 1998

KESTX03 is a single chip ASK (Amplitude Shift Key) transmitter IC. It is designed to operate in a variety of low power radio applications including keyless entry, general domestic and industrial remote control RF tagging and local paging systems.
The transmitter offers a high level of integration and performance.

The basic architecture utilises a crystal reference oscillator, an integrated frequency multiplying PLL and a power output stage. The design is centred around the popular 433.92MHz operating frequency and particular emphasis has been placed on low current drain, including a power–down feature which greatly increases battery life.

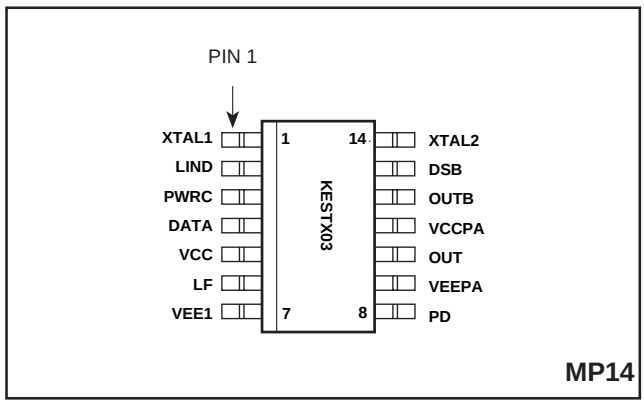

Figure1 Pin connections - top view

FEATURES

- Low supply Current
- Full Power down feature
- Adjustable output power level
- Low external part count
- Fully integrated VCO, PLL and Power Amplifier
- On-frequency flag (PLL lock indicator)
- 2 V operation
- PA/VCO interlock prevents unwanted transmission

ABSOLUTE MAXIMUM RATINGS

Supply voltage	V_{EE} -0.5 to TBA
Storage temperature	-55 to +150°C
Junction temperature	-55 to +150°C
Voltage on any pin	V_{EE} -0.5 to V_{CC} +0.5 V

ORDERING INFORMATION

KESTX03/KG/MPAD (Tape and Reel)
KESTX03/KG/MPAS (Tubes)

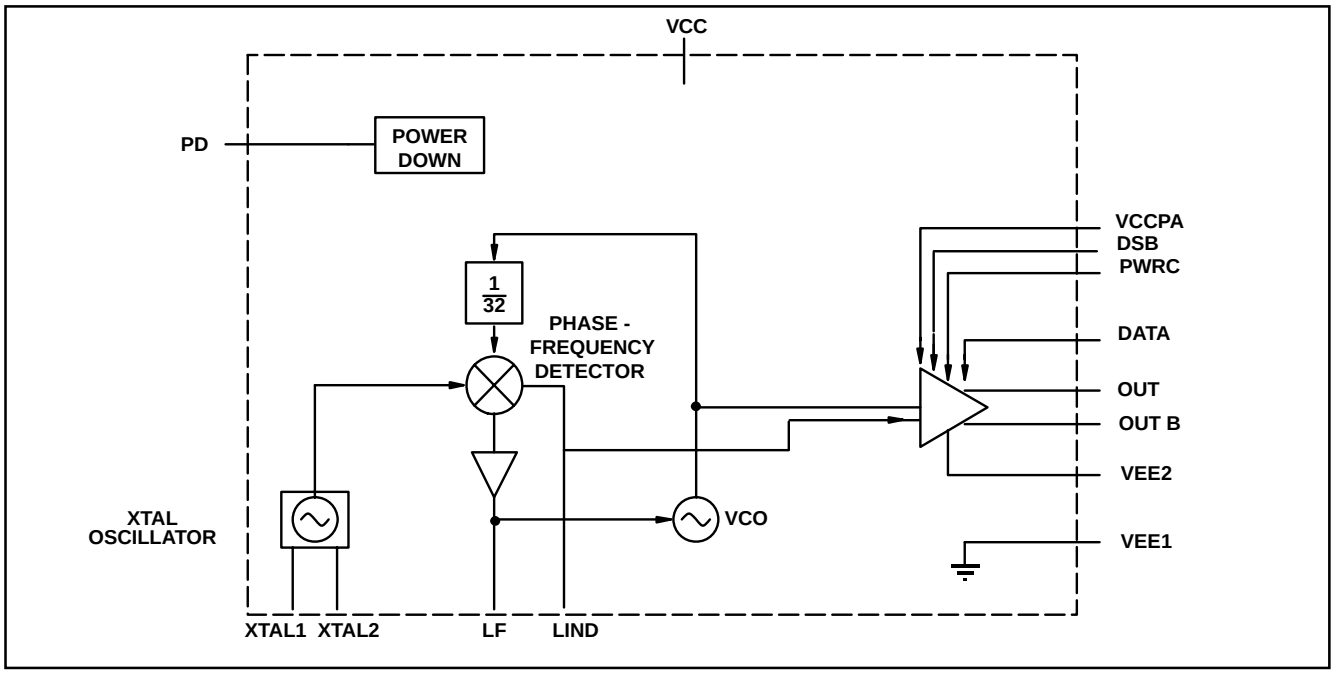

Figure 2 block diagram

ELECTRICAL CHARACTERISTICS Operating conditions

These characteristics are guaranteed over the following conditions (unless otherwise stated):

T_{AMB} = -20°C to +85°C, V_{CC} =2.0V to TBA. These characteristics are guaranteed by either production test, characterisation and or design. They apply within the specified ambient temperature and supply voltage ranges unless otherwise stated.

Parameter	Symbol	Value			Units	Conditions
		Min	Typ	Max		
Power Supply voltage	V_{CC} KG	2.0		TBA	V	
Ambient temperature	T_{AMB} KG	-20		85	°C	

ELECTROSTATIC PROTECTION

Standard ESD protection has been applied to all pins to meet the 2kV all pins - human body model

ELECTRICAL CHARACTERISTICS DC

These characteristics are guaranteed over the following conditions (unless otherwise stated):

T_{AMB} = -20°C to +85°C, V_{CC} =2.0V to TBA. These characteristics are guaranteed by either production test or design

Parameter	Symbol	Value			Units	Conditions
		Min	Typ	Max		
Supply current standby mode	$I_{CC}1$			5	µA	PD= 0V; V_{DATA}=0V Low
Supply Current PLL enable/transmit space	$I_{CC}2$			5	mA	PD= High; VCC = 2.0V (PA OFF)
Supply current PLL enable/transmit mark	$I_{CC}3$			TBA	mA	PD = High; V_{CC} = 2.0V RF power into 50Ω; -TBA
Supply current PLL enable/transmit space Supply current	$I_{cc}4$			5	mA	PD = High V_{CC} =TBA
PLL enable/transmit mark	$I_{CC}5$			TBA	mA	V_{CC} = TBA, 434MHz PD = High; RF power into 50Ω=TBA
PD transmit enable	V_{PDH}	V_{CC} -0.5		V_{CC}+0.2	V	
PD transmit	V_{PDL}	V_{EE} -0.2		0.5	V	
PD input bias current	I		TBA		µA	PD voltage = TBA
Data pin input logic high	V_{ih}	$0.7V_{CC}$		V_{CC}+0.5	V	I_{INI} = +100µA (Max)
Data pin input logic low	V_{il}	V_{EE} -0.3		$0.5V_{CC}$	V	I_{INI} = -100µA (Max)

Notes:- The maximum supply is directly related to Imod and hence the output power level.

ELECTRICAL CHARACTERISTICS DC

These characteristics are guaranteed over the following conditions (unless otherwise stated):

T_{AMB} = -20°C to +85°C, V_{CC} =2.0V to TBA. These characteristics are guaranteed by either production test, characterisation or design. They apply within the specified ambient temperature and supply voltage ranges unless otherwise stated.

Parameter	Symbol	Value			Units	Conditions
		Min	Typ	Max		
Output power into 50Ω at fundamental (see note 1)	PFR_P	TBA	-10	TBA	dBm	Rp=TBA; F_O=434MHz V_{CC} = 2.0V; Fo
Output power into 50Ω at fundamental (see note 1)	PFR_P	TBA	0	TBA	dBm	Rp=TBA; F_O=434MHz V_{CC}=2.0V
Output power into 50Ω at fundamental (see not 1)	PFR_P	TBA	0	+10	dBm	Rp=TBA F_O=434MHz V_{CC} = TBA
Output power at 2 x fundamental into 50Ω (see notes 1 & 2)				TBA	dBc	Rp = TBA; F_O = 434MHz
Output power at 3x fundamental and all other spurii into 50Ω (see note)				-11	dBc	Rp = TBA; F_O = 434MHz
Phase detector gain	PDG		16		µA/rad	
Extinction ratio (see note 3)	ER	40			dB	
VCO gain	G_{VCO}	70	260	450	MHz/V	
PDH settling time (see note 4)	Txe			5.0	ms	
Output sidebands due to reference frequency (see note 5)	SB		-40		dBc	F_O = 434MHz
30dB Data Pulse rise time	T30R		380		ns	When keyed set externally C 6 = TBA
30dB Data pulse fall time	T30F		430		ns	
VCO operating frequency		TBA	434	TBA	MHz	
Lock Detect High	LDH	V_{CC}-0.3			V	I = TBA µA
Lock Detect Low	LDL			V_{EE} + 0.3	V	I = TBA µA
Max Data Rate			100		KBits/s	
Tx output phase noise at 1MHz offset	PHNZ		-85		dBc/Hz	see Table (page 5)

Notes:

1 Limits can only be established after full characterisation of the part.

2 The spurii are specified relative to the fundamental measured in a 300KHz resolution bandwidth

3 Extinction ratio is defined as the ratio of the output power for (SPACE) to output power for (MARK) measured at the output operating frequency.

4 Regulatory issues demand that transmission does not take place until the PLL has acquired lock and the VCO is operating at its final output frequency. This requirement demands that pin LIND is set high at least Txe ms prior to the transmission of any data. This value is dependent on the PLL loop bandwidth and hence on the value of the external loop filter component values. The specification value above is for the loop filter components shown in the applications diagram (Figure 5)

5 Sidebands on the output due to the PLL reference are a function of the PLL loop bandwidth and the application. Reducing the closed loop bandwidth of the PLL loop will aid in reducing the level of the reference spurii.

PIN LISTING

Signal	Description	Signal	Description
XTAL1	Crystal oscillator	LIND	Lock indicator
XTAL2	Crystal oscillator	PWRC	Output Power Control
DATA	Input data	VCCPA	Power amplifier positive supply
PD	Power Down/Power up	VEEPA	Power amplifier ground
OUT	Power amplifier output/antenna interface (complemenary output)	VEE1	PLL ground
OUTB	Power amplifier output/antenna interface (complentary output)	VCC	Positive supply
LF	Phase detector output	DSB	Data sideband suppression

DESCRIPTION

When the IC is enabled a phase locked loop locks the output of the VCO to a multiple of a crystal reference input. The output of the VCO operates at the final output frequency and is the input to a power amplifier stage. The power amplifier directly drives the antenna.

The DSB pin allows control of the rise and fall times of the envelope.

RF Oscillator

The RF oscillator consists of a VCO locked to a crystal oscillator using a phase locked loop (PLL). This consists of a divider, phase detector frequency reference and a loop filter.

Dividers

A divide by 32 prescaler is present in the PLL feedback loop. The final output frequency is thus Fo=32x Fref. e.g.

$$XTAL = \frac{433.92MHz}{32} = 13.56MHz$$

Phase detector

The phase detector used is a phase frequency detector (PFD) with a current (charge pump) output. This phase detector has a triangular characteristic for an input phase error, θe, in the range $-2\pi < \theta e < 2\pi$. The charge pump provides an output current in the range $\pm$ 100μA and hence gives a phase detector gain of (100/2π) μA/rad (16μA).

The advantage of the PFD over a pure phase detector is that it is also a frequency discriminator and will always lock the loop irrespective of the initial frequency offset. The PLL loop characteristics such as lock–up time, capture range, loop bandwidth and VCO reference sideband suppression are controlled by the external loop filter (C3, C2 and R2).

For certain applications spurious sidebands at the reference frequency must be adequately suppressed and so a 3rd order loop is recommended.

VCO

To minimize external component costs the VCO is fully integrated. The frequency of the VCO is controlled by the voltage on pin LF.

Reference crystal oscillator

A single transistor Collpits crystal oscillator provides a reference clock for the PLL.

The oscillator is configured for parallel resonant operation in the fundamental mode (typical operating frequency of 3–7MHz) and the crystal used should be specified for a specific parallel load capacitance. The crystal is connected between pins XTAL2 and VEE1with external components as shown in Figure 5.

Alternatively, a reference clock can be provided by an external source ~200mV p-p, a.c. coupled into pin XTAL2.

Output stage (PA)

The input signal at pin DATA produces ON OFF Keying (OOK) modulation of the VCO frequency output at pins OUT and OUTB. This is achieved by on–off keying of the bias current in the output power amplifier stage. The output of the PA is a balanced output (pin OUT and OUTB) and is current source driven (open collector outputs). The outputs of which should be D.C. referenced to a positive supply voltage (anticipated to be V_{CC} in most applications). The current source outputs can drive a PCB antenna directly (Figure 5) or if a higher output power is required on limited supply headroom via a simple impedance transforming network. A balanced output stage is used as it automatically suppresses the even order harmonics of the fundamental. Of particular importance for the European application is suppression of the 2nd harmonic (due to regulatory issues concerning spurious outputs). In order to obtain the benefits of this output stage it is essential to use a balanced antenna.

Power up

In the intended application it is expected that the transmitter will spend a large proportion of time in ‘‘stand by” not transmitting data. To maximise battery life it is important that very little quiescent current is taken in this mode.

The ‘‘stand by mode” is selected by setting pin PD LOW and similarly the transmitter is enabled by setting PD HIGH. The voltage on PD should not exceed V_{CC} by more than 0.2Volts.

From an application standpoint the PD pin should be decoupled to prevent high frequency noise directly coupling into the IC power supply. Since PD enables the PLL it is essential that it is set high prior to any data transmission and that it remains high during the transmission. There are three different power drain modes:

(i) Stand by (PD LOW, DATA LOW)
(II) PLL Mode/Transmit SPACE (PD HIGH, DATA LOW)
(III) Transmit MARK (PD HIGH, DATA HIGH)

Phase noise and occupied bandwidth requirements (to be confirmed)

Frequency Offset from Carrier	Phase Noise dBc/Hz Data Rates
KHz	1KB/s
12.5	-66
20	-76
25	-86
40	-86
50 and greater	-86

APPLICATIONS INFORMATION

Power control

The bias current for the power amplifier directly controls the output current (and hence the output power). The bias current is set by the external resistor connected between PWRC and ground.

The bias voltage on pin PWRC is nominally 1.20V and hence the modulation current Imod is given by 1.20/R.
To a first order neither the linearity (harmonic spurii relative to fundamental) or the amplifier efficiency are affected by Imod. the graph below shows typical simulation results for the amplifier current output with Imod variation.

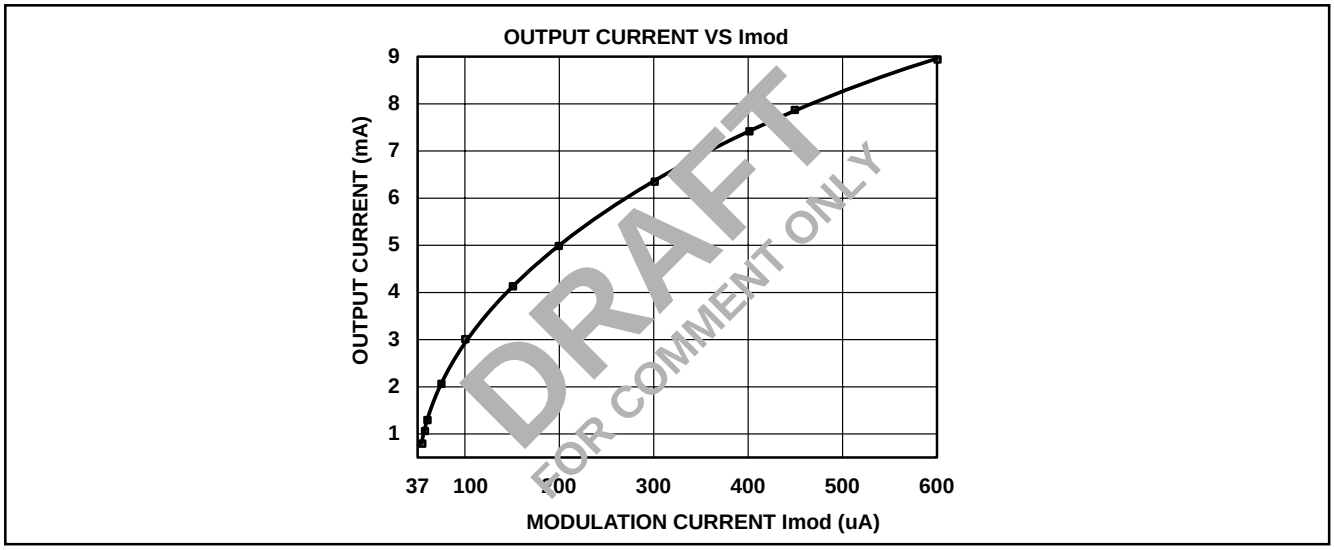

Figure 3 PWRC power control

Frequency accuracy

The stability of the output frequency is equal to that of the crystal referenced oscillator and shift in the VCO frequency during data modulation. To operate with a final output accuracy of ± 66KHz at 433.92MHz (as required for use with the receiver KESRX01) would require a crystal with a tolerance specification of ± 150ppm. This tolerance should encompass e.g. initial accuracy, temperature stability and ageing.

Operation at a final output frequency of 433.92MHz requires a crystal specified for operation at 13.56MHz.

Antenna interface

The IC is capable of directly interfacing to a PCB loop antenna as shown in the applications diagram (Figure 5)

Figure 4 is an equivalent circuit for a PCB loop antenna. The inductance of the loop is Lant and this is in series with two resistors. These represent Rr the radiation resistance and Rs the series resistance of the antenna.

The Q of the antenna is defined as(ωo*Lant/(Rs+Rr)) where ωo is the resonant frequency (rad/s) of the antenna.

At resonance the antenna can be transformed to the equivalent circuit on the right hand side (Figure 4). Here the equivalent parallel resistance Rp is given by

$$Rp = (Rs + Rr)(Q\ 2 + 1)$$

For example, Ls=40nH, fo=433MHz, (Rs+Rr)=2.2 , Q=50, gives an equivalent parallel resistance of 5.4kΩ.

Typically the antenna will be d.c. referenced to VCC as shown in the applications diagram. The maximum voltage swing across the antenna is therefore limited by the RF saturation voltage of the output PA stage. This is of the order of 0.5V and hence the peak to peak voltage across the antenna will be 2*(VCC–0.5V) e.g. 9V for Vcc=5V. This means that the maximum current that can be driven into the load is 1.7mA (peak–peak at the fundamental) and the external power control resistor should be set accordingly.

If it is necessary to drive more power into the antenna a possible way to accomplish this is to perform an impedance transformation to the antenna.

The antenna also acts as a filter on unwanted harmonic spurii. The use of a balanced output suppresses the 2nd harmonic (and other even order harmonics).

The 3rd harmonic of the fundamental is not automatically suppressed. However even a Q as low as 10 will reduce the 3rd harmonic by a further 32dB relative to the fundamental.

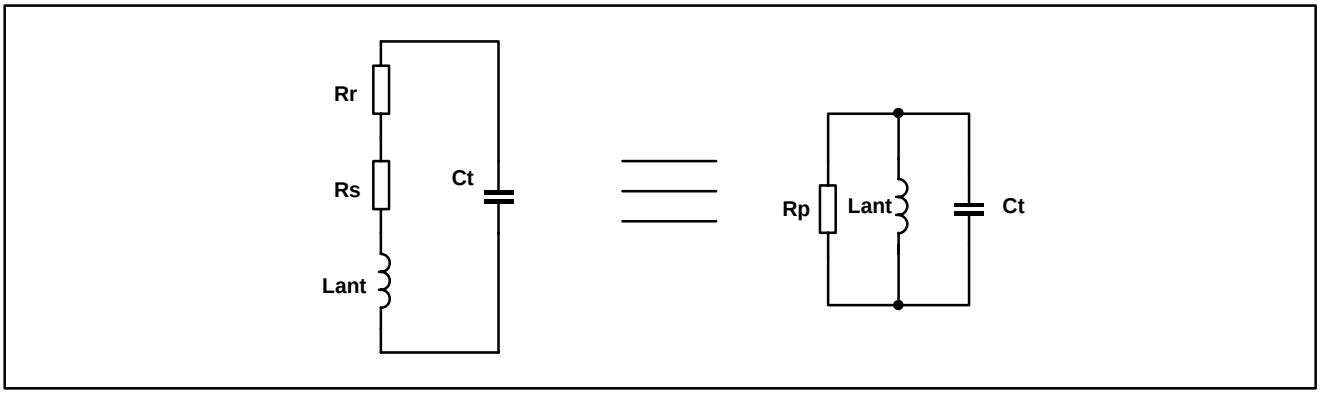

Figure 4 Loop antenna

Note: The following application diagram is provided to assist the customer in using the IC. No guarantee can be made as to its correctness.

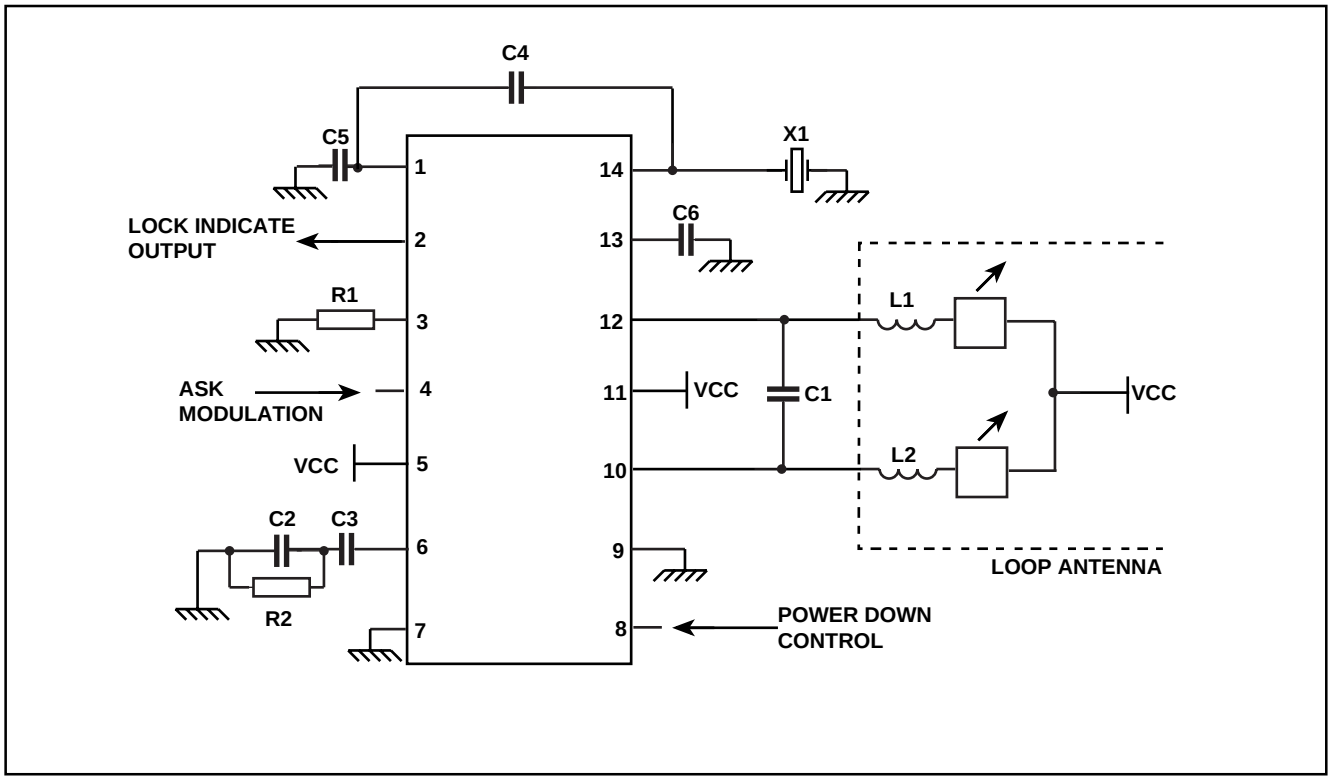

Figure 5 Application diagram

COMPONENT LIST at 433.92MHz

COMPONENTS	FUNCTION	VALUE	UNITS
R1	Output Power Control	TBA	kΩ
R2	PLL Loop Filter	TBA	Ω
C1	Antenna Tuning	Application Dependent	pF
C2	PLL Loop Filter	TBA	nF
C3	PLL Loop Filter	TBA	nF
X1	Parallel Resonant Crystal	13.56	MHz
C4	Crystal Oscillator	18	pF
C5	Crystal Oscillator	18	pF
C6	Data Side Band Control	TBA	pF
L1 and L2	Antenna tuning	Application dependent	nH

TESTABILITY REQUIREMENTS

This section is a summary of the observability and controllability requirements identified to simplify the production test requirements of the device.

1. Ability to directly drive XTAL oscillator from the tester (no crystal). The XTAL2 pin allows direct drive of the oscillator with an external clock source as shown in Figure 6. Typically a 200mVp clock signal is AC coupled to produce differential output on OP and OPB. (C=10nF, Rs (Source) <5k)

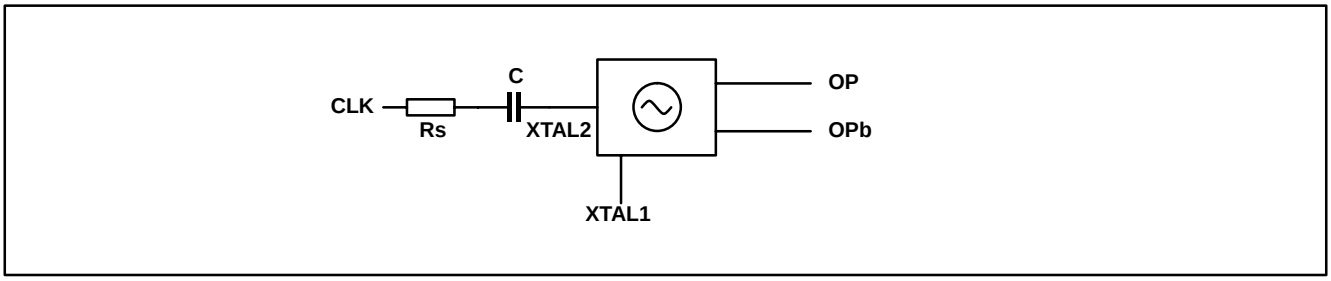

Figure 6 Direct drive of crystal oscillator

2. Control of the VCO frequency is obtained via the LF signal pin. The output of the dividers is tested by measuring the DC current output of the charge pump (with XTAL2 held at VCC).

3. DC operation of the power amplifier is observed by measuring the current through the open collector outputs OUT and OUTB.

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